Proceedings of the World Congress on Electrical Engineering and Computer Systems and Science (EECSS 2015)
Barcelona, Spain – July 13 - 14, 2015
Paper No. 137

A Study on the Characteristics of a Temperature Sensor with an Improved Ring Oscillator

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Abstract- This paper presents low power and high speed on-chip temperature sensor that uses only two ring oscillators which have different CMOS delay characteristics, counters and Time-to-Digital Converters (TDC) to maintain the performance benefit of the CMOS digital circuit. This novel temperature sensor does not require any bias circuits or external reference clocks. It measures the delay variations between the temperature-sensitive signal generator and the temperature-insensitive signal generator according to the temperature. The two ring oscillators were designed for the different gate channel length CMOS inverter. Additionally, the temperature-sensitive ring oscillator was stacked on the Cascode CMOS inverter. It generated two signals which were sensed by the TDC. However, temperature sensor of TDC cells, which was used to measure the delay time of two CMOS delay characteristics and convert to digital outputs, occupied a large chip area. To overcome this problem, we designed an advanced temperature sensor using Coarse-Fine TDC. We checked the performance of the temperature sensor using a HSPICE simulation.

***Keywords*:** Time-to-Digital Converter, Temperature Sensor, Ring Oscillator, Propagation Delay Time

1. Introduction

Currently, the huge demand of mobile devices requires a very large amount of CMOS on the Chip. The reduction of the channel length through scaling down has brought the decrease of gate delay by approximately 30% each generation. Therefore, the performance of the circuits associated with the operating speed has been continuously improved. Consequently, the increase of transistors has brought the increase of heat generated by the IC Chip. Heat generated in the IC Chip induces the temperature rise in the Chip. This causes a large amount of power being consumed and also results in low reliability of IC Chip. Therefore, On-Chip temperature sensors are needed to monitor the temperature variation of devices.

Conventional band-gap temperature sensors which consist of substrate bipolar transistors and an Analog-to-Digital Converter(ADC) have been widely used in CMOS VLSI systems. In addition, the CMOS temperature sensors using ring oscillator or inverter delay lines have been proposed, because they occupy a small area, have a simple design, and provide a higher resolution as shown by P.Chen et al(2005) and Dongwan Ha et al(2012). Additionally, using the two ring oscillator rather than using a one ring oscillator also results in a higher resolution as shown by Hokyu Lee et al(2010). The delay differences between an inverter delay line and a reference delay line are compared using a delay sensing scheme. This paper presents a low cost all-digital temperature sensor using two ring oscillators which have different temperature characteristics. In order to obtain a higher resolution, we adjust the gate channel length and stacked to Cascode CMOS inverters which consist of ring oscillator. The difference between the two clocks can be amplified using counters as shown by Jinse Kim et al(2015). In this paper, by increasing the maximum delay difference due to the temperature of the two delay lines, the temperature sensor is proposed as a method which results in a higher resolution.

2. Analysis Model of the Temperature Sensor

The proposed temperature sensor is divided into a clock generator circuit and a clock detection circuit. In this paper there is a proposed temperature sensor with a high resolution using the control of the gate channel length and stacked Cascode stage of the ring oscillator in clock generator circuit.

2. 1. Design of the Clock Generator Circuit

Conventional CMOS temperature sensors typically have reference sources, such as reference delay lines or external clocks. However, the use of external clocks as the reference source are not only sensitive to the external noise but also cannot be applied to some applications having various operating frequencies. To overcome the disadvantages of an existing reference clock generator, a reference clock generator circuit can be used, as shown in Fig. 2.1.

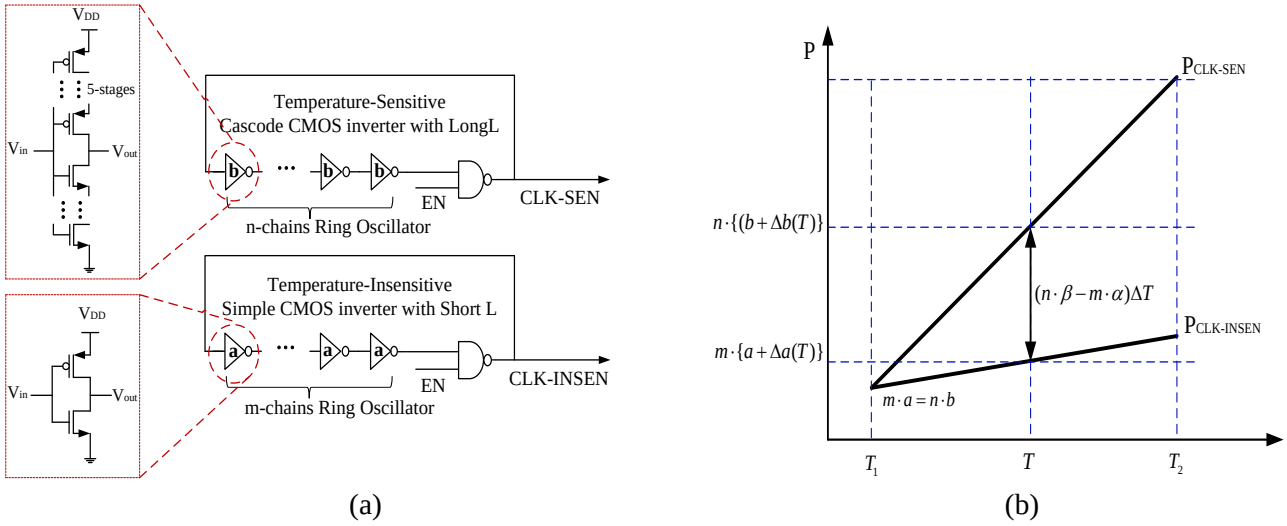

Fig. 2.1 Clock generator circuit
(a) Schematic of clock generator with ring oscillator
(b) Clock delay of ring oscillator for temperature

The upper-part of the ring oscillator in Fig. 2.1(a) is composed of a temperature-sensitive ring oscillator, and the lower-part is composed of a temperature-insensitive ring oscillator. When the operating temperature is increased to T from T_1, it is assumed that increase of the delay time of each inverter by Δa(T), Δb(T). In order to compare the period of both clocks, we set the reference point of T_1 is at least the operating temperature. Therefore, the period of the dual ring oscillator at T_1 is the same. As shown in the following equation (1).

$$\Delta P(T_1) = P_{CLK-SEN}(T_1) - P_{CLK-INSEN}(T_1) = 0$$
$$\therefore \mathrm{m} \cdot \mathrm{a}(0) = \mathrm{n} \cdot \mathrm{b}(0) \quad (1)$$

Delay time is linearly proportional to the temperature variation in the inverter. A delay time variation in the insensitive inverter and sensitive inverter to temperature variation can be set at respectively α and β. Therefore ΔP(T) can be expressed by a linear function of the temperature variation, as in equation (2).

$$P(T) = n\Delta b(T) - m\Delta a(T) = (\mathrm{n} \cdot \beta - \mathrm{m} \cdot \alpha)\Delta \mathrm{T}, \quad \text{where } \Delta a(T) = \alpha,\ \Delta b(T) = \beta \quad (2)$$
$$\therefore P(T) \propto \Delta T \quad (3)$$

It can obtain the temperature sensor with a high resolution by making a large the difference between α and β, as shown in equation (3). Therefore, it is possible to control a channel length and a Cascode stage ring oscillator, as it was proposed as a method which can increase the difference between these clocks period in the next section.

2. 1. 1. Variation Rate of the Propagation Delay along the Channel Length

A temperature sensor with a higher resolution has larger values of ΔP(T) at the same temperature, since it is necessary to design a temperature-sensitive ring oscillator which has a maximum β and temperature-insensitive ring oscillator which has a minimum α, as shown in Equation (3). In order to design a ring oscillator with a minimum α and maximum β, we propose a method for changing the gate channel length of a CMOS inverter.

When increasing the NMOS gate channel length of a CMOS inverter, it is increased that the absolute magnitude of the delay time. This not only decreases the drained current when the gate channel length is increased, but the load capacitance is also increased. Additionally, the temperature dependence of the delay time of the CMOS inverters is the main design factor of the CMOS temperature sensor, since the mobility of CMOS transistors varies with temperature. Neutral scattering occurs due to collisions between carriers and structural defects which are generated by pocket implantation or channel doping implantation in LDD MOSFET. Structural defects already formed such as point defect, dislocation are independent with temperature. So, neutral scattering is independent to temperature variations. Pocket implantation area is identical regardless of gate channel length. But the structural defects zone which is generated by high implantation energy is large for such a short channel MOSFET in relation to gate channel area. Therefore, neutral scattering is a main factor to determine the carrier mobility on MOSFET with short gate channel lengths as shown in Fig. 2.2, by Cros.A et al(2006). The propagation delay of a inverter is inversely proportional to the carrier mobility as shown by Demassa T A et al(1996). The temperature dependent delay varies according to the gate channel length of MOSFET. As shown in Fig. 2.2, it is possible to know the mobility of the relationship between the NMOS gate channel length.

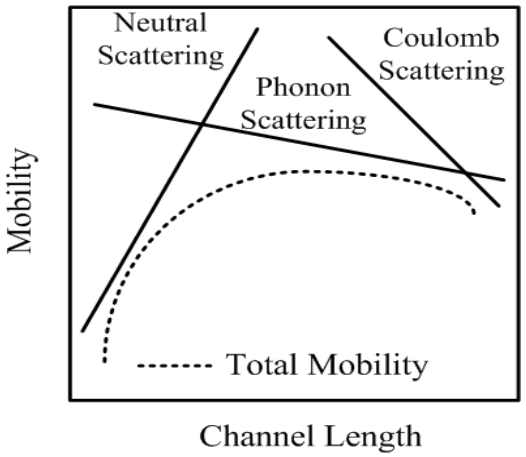

Fig. 2.2. Mobility due to NMOS Gate Channel Length, as shown by Shin-ichi Takagi et al (1994)

By increasing the gate channel length of the NMOS, the variation rate of the delay time is increased due to temperature variation.

2. 1. 2. Variation Rate of the Propagation Delay along the Cascode Stage

Secondly, a method is composed for the stacked up Cascode stage where the design of a CMOS ring oscillator has a minimum α and maximum β. The Cascode inverter, whose transistors have stacked up as shown in the upper-part of Fig. 2.1(a). Propagation delay time in the basic CMOS inverter can be expressed in the following equation (4) by P.Chen et al(2005).

$$t_p = \frac{t_{pHL}+t_{pLH}}{2} = \frac{(L/W)C_L}{\mu C_{ox}(V_{DD}-V_T)} ln\left(\frac{1.5V_{DD}-2V_T}{0.5V_{DD}}\right) \quad (4)$$

However, in the case of the Cascode CMOS inverter, it is not possible to use the equation (4). The source node of the PMOS connected to a basic CMOS inverter is immediately applied external supply voltage V_{DD}. Additionally, the source node of the NMOS connected to the output stage is connected directly to the ground. However, PMOS and NMOS of Cascode CMOS inverter is connected through the n number of PMOS and NMOS. Therefore, there will be a reduction in V_{DD} and because of the use of n NMOS and n PMOS, there is a large parasitic capacitance than the basic CMOS inverter. Parasitic capacitance causes an increase in the load capacitance C_L by equation (4).

$$t_p = \frac{t_{pHL}+t_{pLH}}{2} = \frac{(L/W)C_L}{\mu C_{ox}(V_{DD}-\Delta V-V_T)} ln\left(\frac{1.5V_{DD}-\Delta V-2V_T}{0.5V_{DD}-\Delta V}\right) \quad (5)$$

As a result, it can be represented through the modeling equation as an approximatation of equation(5). Therefore, the proportion of threshold voltage V_T in section $(V_{DD} - \Delta V - V_T)$ is increased due to the reduction of a Cascode CMOS inverter V_{DD}. The threshold voltage decreases as the temperature increases, the Cascode CMOS inverter is to have a large propagation delay time than the basic CMOS inverter. Since the variation rate of the delay time is increased due to increase in the Cascode stage, it is possible to increase the β value accordingly.

$$\alpha \propto (Channel\ Length)^{-1} \propto (Cascode\ stage)^{-1} \quad (6)$$
$$\beta \propto (Channel\ Length) \propto \text{Cascode stage} \quad (7)$$

Consequently, the above equations (6) and (7), can be modelled for α and β. Therefore, the temperature-insensitive CMOS ring oscillator satisfied the equation (6) by the channel length using short CMOS inverters with the value of minimum α. Furthermore, the temperature-sensitive CMOS ring oscillator satisfied equation (7) by the long channel length Cascode CMOS inverter that has a maximum value β. This makes it possible to select the CMOS ring oscillator with a minimum α and maximum β value. As a result, a temperature sensor with a higher resolution is proposed.

2. 2. Design of the Clock Detection Circuit

In this section, we explain how the clock detection circuit was used to converts a delay difference between both clocks to the digital code. It is amplified by $(n \cdot \beta - m \cdot \alpha)$ from equation (2). The difference of the periods of both clocks can be converted by using TDC to digital code.

It was designed by dividing the conventional TDC to Coarse-TDC and Fine-TDC as presented in Fig. 2.3, as shown by Jinse Kim et al(2014). The Fine-TDC can detect at a rate of 1a per D-flipflop using 11 delay cells with the minimum channel length. Accordingly, the coarse-TDC, consisting of 11 times the fine delay cells in the Fine-TDC, is used to detect at a rate of 11a per bit, where n is 11. Therefore, the clock detection circuit is configured by the number of n Coarse-TDC and Fine-TDC which has a time difference between 144a for $(n+1)^2$ bits in the digital code which can be converted, as shown in Fig. 2.3. A two-step TDC, which consists of a coarse-TDC and a fine-TDC, is used in order to minimize the chip area and reduce the number of D-flipflop.

Therefore, it is possible to design a temperature sensor which has a smaller chip area and a high resolution. Since CLK-SEN and CLK-INSEN passed the counter are composed of a total of n stages, the period of each clock is amplified in 2^n times. Thus, $\Delta T_D(T)$ is the difference of the period of CLK-INSEN-C and CLK-SEN-C at any temperature T that can be expressed as an equation (8).

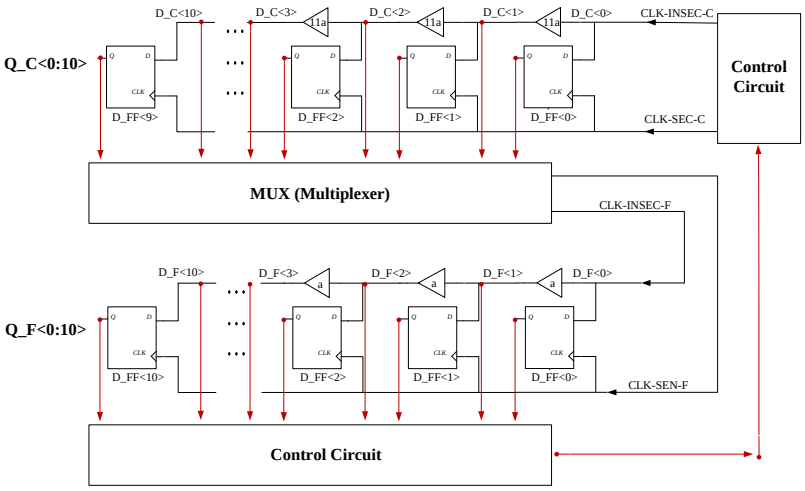

Fig. 2. 3. Design circuit of the Coarse-TDC and Fine- TDC

$$\begin{aligned}\Delta \boldsymbol{T_D}(\boldsymbol{T}) &= \boldsymbol{T_{D,CLK-SEN,Coarse}}(\boldsymbol{T}) - \boldsymbol{T_{D,CLK-INSEN,Coarse}}(\boldsymbol{T}) \\ &= 2^x \cdot n \cdot \{b + \Delta b(T)\} - 2^x \cdot m \cdot \{a + \Delta a(T)\} \\ &= 2^x \cdot n\Delta b(T) - m\Delta a(T) \end{aligned} \quad (8)$$

$\Delta \boldsymbol{T_D}(\boldsymbol{T})$ is converted in the Coarse, and Fine-TDC block to digital code. The number of delay cells on each of the two delay paths is decided in terms of m and n in the following equations (10) and (11).

$$\mathrm{ma}(0) = \mathrm{nb}(0) \qquad \text{at } T = 0℃ \quad (10)$$

$$2^{\mathrm{x}} \cdot \{\mathrm{n}\Delta \mathrm{b}(\mathrm{T}) - \mathrm{m}\Delta \mathrm{a}(\mathrm{T})\} > 144a \qquad \text{at } T = 100℃ \quad (11)$$

The proposed temperature sensor can be designed as a clock generator circuit and clock detection circuit. In the next chapter, it was verified through a simulation of the temperature sensor with a high resolution.

3. Simulation Results

First, in order to satisfy the presented minimum and maximum conditions in the previous chapter, we simulated two variables.

(a) Increase in delay time variation due to the increase of the NMOS channel length
(b) Increase in delay time variation due to the increase of Cascode stage

The simulation in (a) was the propagation delay time of the CMOS inverter when changing the operating temperature of from 0 ℃ to 100 ℃ and increasing the gate channel length of the NMOS. Gate channel length of the NMOS has designed a CMOS inverter of 3.50μm from 0.11μm. In addition, the operating temperature was changed from 0 ℃ to 100 ℃, which was performed to simulate the inverter delay time. During this time, the gate channel length of PMOS was fixed at 1.2μm. Fig. 3.1 shows normalized propagation delay versus temperature at different channel lengths in 0.11μm process. The inverter with the long channel length has a large delay variation and the short channel length has a small delay variation as shown Fig. 3.1.

Therefore, the channel length of a CMOS inverter for the temperature-insensitive ring oscillator was selected by 0.11μm, which had a 9.62% variation rate of delay time. Moreover, CMOS inverter for the temperature-sensitive ring oscillator had a maximum β, when the channel length was 3.50um, which had a 31.62% variation rate of delay time. It shows the variation rate of the largest delay time. However, in order to obtain a high resolution, a large variation rate of the delay time is required.

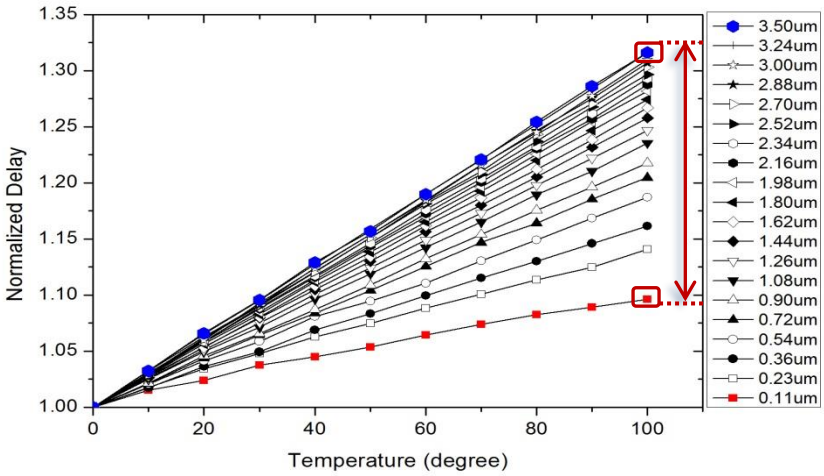

Fig. 3.1. Normalized propagation delay versus temperature in 110nm process.
$\mathrm{dD(T)}/dT$ increased according to gate channel length.

Therefore, through an increased in not only the channel length but also the Cascode CMOS inverter stages, we have designed a CMOS inverter for the Cascode stage from 2 stages to 15 stages about Dongbu 0.11μm process. Additionally, when changing the operating temperature from 0 ℃ to 100 ℃, it was simulated for a propagation delay time of the Cascode CMOS inverter. As shown in Table. 1, the rate of variation of the delay time associated with Cascode stage increases.

Table. 1. Variation rate of the delay time at 100 ℃ from 0 ℃ in the Cascode stage

Cascode CMOS Inverter stage (Channel Length=3.50μm)	Variation rate of the delay time(%)
1	31.62
2	38.09
3	39.84
5	40.32
10	40.35
15	40.41

As a result, the temperature sensitive ring oscillator was selected in Cascode CMOS inverters of 5 stages of the gate channel length 3.5um. The 5 or more stage Cascode CMOS inverter, the varation rate of the delay time was saturated. In addition, because it requires a large-scale V_{DD} voltage, Cascode CMOS inverters of 5 stages is appropriate. Therefore, it was based on the above simulation results, to select the inverter. Furthermore, it was designed with m and n values which satisfies the condition of equation (1), as shown in Table. 2.

The difference in the delay time variation rate of the proposed temperature sensor and conventional temperature sensor is shown in Fig. 3.2. The conventional temperature sensor, temperature-sensitive ring oscillator was configured using a CMOS inverter. Additionally, temperature insensitive ring oscillator was used as a reference clock [2]. As shown in Fig. 3.2, it is compared to the variation rate of the delay time for the temperature of the conventional temperature sensor, the proposed temperature sensor has a variation rate of large delay time about 2 times. Thus, the temperature sensor that was proposed in this paper achieves a higher resolution than the conventional temperature sensor.

Table. 2. Design parameters of the CMOS Inverters constituting a ring oscillator

Delay time of 9.62% 1 stage CMOS Inverter			Delay time of 40.32% 5 stage Cascode CMOS Inverter		
NMOS W/L(μm)	PMOS W/L(μm)	m-chains	NMOS W/L(μm)	PMOS W/L(μm)	n-chains
0.64/0.11	0.64/1.2	17	0.64/3.5	0.64/1.2	4

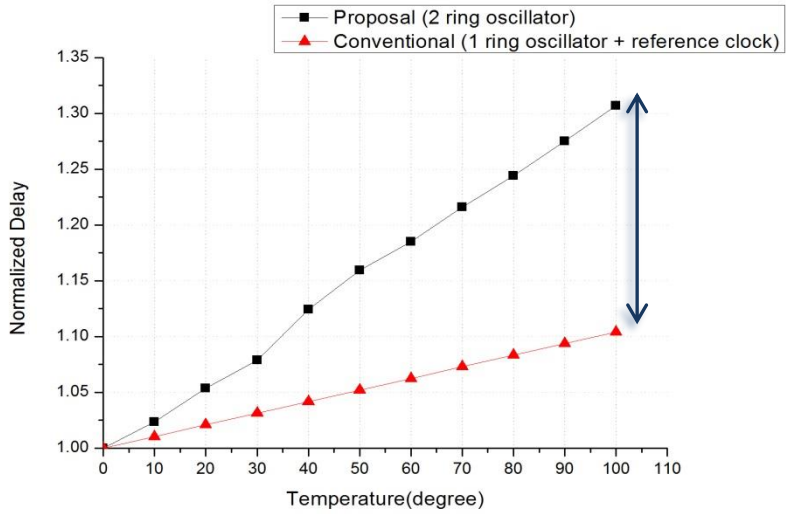

Fig. 3.2. Clock period comparison of the proposed temperature sensor and conventional temperature sensor

4. Conclusion

In this paper, an improved digital CMOS temperature sensor was proposed that does not include the external clock and bias circuit. The proposed temperature sensor needs only a small chip area and has low power consumption without voltage or current bias circuit such as a band-gap reference. In order to design a temperature sensor with a high resolution, the variation rate of the delay time in the gate channel length and Cascode stage was significantly optimized. Additionally, the difference between the two clocks can be amplified using counters. It was then designed by utilizing the difference of the increased clock cycles from the temperature detecting sensor with a high resolution. After we designed on the basis of a temperature sensor with 0.11μm process parameters, we checked the performance of the temperature sensor using a HSPICE simulation.

Acknowledgements

This work was supported by a grant from Korea University and Samsung Semiconductor Research Center of Korea University.

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